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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
08/984,563	12/03/97	MAILLOUX J	95-0653.03

LMC1/1130

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EXAMINER	
KIM,H	
ART UNIT	**PAPER NUMBER**
2751	13

DATE MAILED: 11/30/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
08/984563	Mailloux et al
Examiner	**Group Art Unit**
H. Kim	2751

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE 3 (three) MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☒ Responsive to communication(s) filed on CPA 9/16/99.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 1 1; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 36-39 + 59-69 is/are pending in the application.

Of the above claim(s)_____ is/are withdrawn from consideration.

☐ Claim(s)_____ is/are allowed.

☒ Claim(s) 36-39 + 59-69 is/are rejected.

☐ Claim(s)_____ is/are objected to.

☐ Claim(s)_____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on_____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on_____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number)_____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received:_____.

Attachment(s)

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s)._____

☒ Notice of References Cited, PTO-892

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Interview Summary, PTO-413

☐ Notice of Informal Patent Application, PTO-152

☐ Other_____

Office Action Summary

Detailed Action

Continued Prosecution Application

1. The request filed on 9/16/99 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 08/984563 is acceptable and a CPA has been established. An action on the CPA follows.

2. Claims 36-39 are presented for examination. Claims 59-69 have been added by the amendment. This office action is in response to the Amendment filed on 9/16/99.

3. The status of the related U.S. applications or patents should be updated and/or included as appropriate in the CROSS-REFERENCE TO RELATED APPLICATIONS section and in any other corresponding area in the specification, if any. (e.g., U.S. Patent Application Serial No. ##/###,### filled Sept. 07, 1990, now abandoned; ..., now U.S. Patent #,###,### issued Jan. 01, 1994; or This application is a continuation of Serial Number ##/###,###, filed on December 01, 1990, now abandoned; ...etc.)

4. It is noted that this application appears to claim subject matter disclosed in the co-pending section of this application. Applicants are reminded to maintain a clear line of demarcation between this application and co-pending applications to avoid possible double patenting.

Claim Objections

5. Claims 60-62, 64-65, and 68 are objected to because of the following informalities:

As to claim 60, It appears that claim 60 does not further limit the subject matter of a previous claim. In line 2, it appears that "a" should be changed to --said--, both first and second occurrences.

As to claim 61, It appears that claim 61 does not further limit the subject matter of a previous claim. In line 2, it appears that "a" should be changed to --said--, both first and second occurrences.

As to claims 62 and 64, It is unclear what "the operations are performed in a different order" is referring to. Examiner assumes that the operations is referring to read and write operations. It appears that there is no support in the specification for "the operations are performed in a different order".

As to claim 65 line 9, it appears that "the first" should be changed to --a first--.

As to claim 68, it appears that there is no support in the specification for "data transfer direction selection in a memory".

Appropriate correction is required.

6. Claims 59-69 are objected to under 37 CFR 1.75(b) as not substantially differing from claims 36-39.

The claims as written do not appear to be substantially different or to provide substantially

different patent protection.

Applicants are required to 1) cancel the objected to claims,(2) amend the claims so that they are substantially different from any other claims, or (3) provide sufficient reasons why the claims as presently written are substantially different or provide substantially different patent protection. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 36-39 and 59-69 are rejected under 35 USC § 103(a) as being unpatentable over *Manning*, U.S. Patent 5,610,864 in view of *Ryan*, U.S. Patent 5,966,724.

As to claim 59, *Manning* discloses a method of accessing a memory (Fig. 1), comprising: receiving an external row address (Fig. 1 and Fig. 2, ADDR, ROW); choosing whether the memory is in burst (col. 6 lines 14-26 and col. 7 lines 43-54) or an EDO mode of

operation (col. 6 lines 14-26); selecting between a read and a write operation (Fig. 2 /WE, a logic high indicates read and a logic low indicates write operation); and executing a read or write operation (Fig. 2, /WE).

Although Manning discloses pipeline mode, Manning does not specifically disclose a step of choosing a burst or a pipeline mode of operation. However, it was well known in the memory art that the step of choosing a burst (col. 4 lines 25-26) or a pipeline mode of operation (col. 4 lines 21-25) as disclosed by Ryan for the purpose of high data throughput (abstract lines 8-9). It is highly desirable feature in the memory art to achieve fast memory access because it would increase the overall system throughput.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate well known concept of choosing a burst or a pipeline mode of operation of Ryan into the invention of *Manning* because Ryan states that it would achieve high data throughput in the memory.

As to claim 60, *Ryan* further discloses switching between a burst mode and a pipeline mode (col. 4 lines 21-26).

As to claims 61, *Manning* further discloses switching between a read and a write operations (Fig. 2 /WE).

As to claim 62, *Ryan* further discloses the operations are performed in a different order

(Fig. 5 /WE and col. 4 lines 21-26).

As to claim 36, *Manning* discloses a method for accessing an asynchronously access memory (Fig. 1 and EDO constitutes asynchronous memory, col. 6 lines 14-16), comprising the steps of: receiving an external row address to the asynchronously accessible dynamic random access memory accessible storage device (Fig. 1 and Fig. 2, ADDR, ROW); selecting between a burst (col. 6 lines 14-26 and col. 7 lines 43-54) and an EDO mode of operation (col. 6 lines 14-26); selecting between a read and a write operation (Fig. 2 /WE, a logic high indicates read and a logic low indicates write operation); and obtaining a first external column address (Fig. 1 and Fig. 2, ADDR, COLm) .

Although Manning discloses pipeline mode, Manning does not specifically disclose a step of selecting between a burst and a pipeline mode of operations. However, it was well known in the art that the step of selecting between a burst (col. 4 lines 25-26) and a pipeline mode of operations (col. 4 lines 21-25) as disclosed by Ryan for the purpose of high data throughput (abstract lines 8-9). It is highly desirable feature in the memory art to achieve fast memory access because it would increase the overall system throughput.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate well known concept of selecting between a burst and a pipeline mode of operation of Ryan into the invention of *Manning* because Ryan states that it would achieve high data throughput in the memory.

As to claim 37, Ryan further a step of obtaining a second external address subsequent to the first external address in the pipeline mode (col.4 lines 22-27)

As to claims 38, *Manning* further discloses generating internal address (col. 5 lines 51-62 and col. 8 line 67).

As to claims 39, *Ryan* further discloses selecting path way (col. 4 lines 21-26).

As to claim 63, *Manning and Ryan* disclose the invention as claimed in claim 36. *Ryan* further selecting an external address only data path for read write read operation of the pipeline mode (col. 4 lines 21-25) and selecting an initial buffered external address path (col. 1 line 26), generating internal column address (Fig. 1 Ref. 26) for read write read operation of the burst mode (col. 4 lines 25-30).

As to claim 64, *Ryan* further discloses the operations are performed in a different order (Fig. 5 /WE and col. 4 lines 21-26).

As to claim 65, *Manning* discloses a method of operating a memory circuit, comprising: receive a mode select signal(col. 6 lines 14-34); receiving an initial external address (Fig. 1 and Fig. 2, ADDR); selecting a read and a write operation (Fig. 2 /WE, a logic high indicates read

and a logic low indicates write operation); cycling a second enabling signal (Fig. 2 /CAS) ; generating an internal address (Fig. 1 Ref. 26); and receiving an external address on each cycle of the second enabling (non-burst and page mode reads on this limitation, col. 7 lines 44-46). Although Manning discloses changing the mode and pipeline mode and, Manning does not specifically disclose a step of changing the mode select signal to select a pipeline mode of operation while maintaining a first enabling signal in an active state and receiving an external address on each cycle of the second enabling signal. However, it was well known in the art that the step of changing the mode select signal to select a pipeline mode of operation while maintaining a first enabling signal in an active state (Fig. 6 and col. 4 lines 21-25) and receiving an external address on each cycle of the second enabling signal (col.4 lines 22-27) as disclosed by Ryan for the purpose of high data throughput (abstract lines 8-9). It is highly desirable feature in the memory art to achieve fast memory access because it would increase the overall system throughput.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate well known concept of changing the mode select signal to select a pipeline mode of operation while maintaining a first enabling signal in an active state and receiving an external address on each cycle of the second enabling signal of Ryan into the invention of *Manning* because Ryan states that it would achieve high data throughput in the memory.

As to claim 66, *Manning* discloses a method for accessing a memory, comprising: maintaining a first enabling signal in an active state (Fig. 2 RAS); maintaining a mode select signal to select a burst mode of operation (Col. 6 lines 14-34); receiving an initial external address (Fig. 1 and Fig. 2, ADDR, ROW); selecting a read and a write operation (Fig. 2 /WE, a logic high indicates read and a logic low indicates write operation); cycling a second enabling signal (Fig. 2 /CAS); and generating an internal address (Fig. 1 Ref. 26).

Although Manning discloses pipeline mode and, Manning does not specifically disclose a step of switching the mode of operation to a pipeline mode. However, it was well known in the art that the step of switching the mode of operation to a pipeline mode (Fig. 6 and col. 4 lines 21-25) as disclosed by Ryan for the purpose of high data throughput (abstract lines 8-9). It is highly desirable feature in the memory art to achieve fast memory access because it would increase the overall system throughput.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate well known concept of switching the mode of operation to a pipeline mode of Ryan into the invention of *Manning* because Ryan states that it would achieve high data throughput in the memory.

As to claim 67, *Manning* discloses a method for operating a memory, comprising: maintaining a first enabling signal in an active state (Fig. 2 RAS); maintaining a mode select signal to select a burst mode of operation (Col. 6 lines 14-34); selecting a read and a write operation

(Fig. 2 /WE, a logic high indicates read and a logic low indicates write operation); cycling a second enabling signal (Fig. 2 /CAS) ; and receiving a stream of addresses and a cycling a second enabling signal (Fig. 2 /CAS).

Although Manning discloses pipeline mode and, Manning does not specifically disclose a step of changing the mode of operation to a pipeline mode. However, it was well known in the art that the step of changing the mode of operation to a pipeline mode (Fig. 6 and col. 4 lines 21-25) as disclosed by Ryan for the purpose of high data throughput (abstract lines 8-9). It is highly desirable feature in the memory art to achieve fast memory access because it would increase the overall system throughput.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate well known concept of changing the mode of operation to a pipeline mode **of Ryan into the invention of *Manning* because Ryan states that it would achieve** high data throughput in the memory.

As to claim 68, *Manning* discloses a method of data transfer direction selection in a memory, comprising: selecting a read and a write operation (Fig. 2 /WE, a logic high indicates read and a logic low indicates write operation) and selecting a burst or an EDO mode operation (col. 6 lines 14-34).

Although Manning discloses pipeline mode and, Manning does not specifically disclose a step of selecting a pipeline mode; select an external address only path when the pipeline mode is selected;

and selecting an internal buffered external address path and generating internal column address when the burst mode of operation is selected. However, it was well known in the art that the step of selecting a pipeline mode (Fig. 6 and col. 4 lines 21-25); select an external address only path when the pipeline mode is selected (Fig. 6 and col. 4 lines 21-25); and selecting an internal buffered external address path (col. 4 lines 25-27 and col.1 line 25) and generating internal column address (Fig. 1 Ref. 26) when the burst mode of operation is selected (Fig. 6 and col. 4 lines 22-27) as disclosed by Ryan for the purpose of high data throughput (abstract lines 8-9). It is highly desirable feature in the memory art to achieve fast memory access because it would increase the overall system throughput.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate well known concept of selecting a pipeline mode; select an external address only path when the pipeline mode is selected; and selecting an internal buffered external address path and generating internal column address when the burst mode of operation is selected **of Ryan into the invention of** *Manning* **because Ryan states that it would achieve** high data throughput in the memory.

As to claim 69, *Manning* discloses a storage device comprising: mode circuitry (col. 6 lines 14-34) and select circuitry for selecting between a read and a write operation (Fig. 2 /WE, a logic high indicates read and a logic low indicates write operation).

Although Manning discloses changing the mode and pipeline mode and, Manning does not

specifically disclose an external address only path for the pipeline mode; an internal buffered external address path for the burst mode of operation; and pipeline/burst circuitry. However, it was well known in the art that an external address only path for the pipeline mode (col. 4 lines 21-25); an internal buffered external address path for the burst mode of operation (Fig. 6 and col. 4 lines 25-27); and pipeline/burst circuitry (Col. 4 lines 20-27). as disclosed by Ryan for the purpose of high data throughput (abstract lines 8-9). It is highly desirable feature in the memory art to achieve fast memory access because it would increase the overall system throughput.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate well known teaching of an external address only path for the pipeline mode; an internal buffered external address path for the burst mode of operation; and pipeline/burst circuitry of Ryan into the invention of *Manning* because Ryan states that it would achieve high data throughput in the memory.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. USP 5966724, 19991012, Synchronous memory device with dual page and burst mode operations, Ryan, Kevin J.

9. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for

response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

10. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

11. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. § 1.111(c).

12. Applicants are requested to number each line of each claim starting with line number one to provide easier communication in the future.

13. When responding to the office action, Applicant is advised to provide the examiner with

the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

14. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Hong Kim whose telephone number is (703) 305-3835. The Examiner can normally be reached on the weekdays from 8:30 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (703) 305-9712.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

15. **Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks
Washington, D.C. 20231

or faxed to:

(703) 308-9051-2, (for formal communications intended for entry)

Or:

(703) 305-9731 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

hk

HK
Patent Examiner
November 23, 1999

EDDIE P. CHAN
SUPERVISORY PATENT EXAMINER